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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
NGUYEN, HIEP

ART UNIT	PAPER NUMBER
2816	9

DATE MAILED: 08/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,679	MAGOON ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communicati n appears on the cover sheet with the corresp ndence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

In response to the Remarks, the finality of the rejection has been withdrawn.

Specification

The disclosure is objected to because of the following informalities: the connections of the third terminals of the first, second and third transistors for receiving the control signal in claim 6 is not disclosed in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 6-8 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The limitation that the third terminals of first, second and third transistors are configured to receive the control signal, in claim 6, is not disclosed in the specification. Correction and /or clarification is required.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 3, the recitation " the transistor circuit" on line 10 is indefinite because it is misdescriptive because the "a circuit" is connected to the transistor device instead of to the "transistor circuit".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Huijsing et al. (US Pat. 4,678,947).

Regarding claims 1 and 2, figure 2 of Huijsing shows a transistor circuit for implementing a switch, comprising:

a first switch node (T1) configured to connect to an external circuit (not shown);

a second switch node (T2) configured to connect to the external circuit:

a transistor device (Q0) having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal; a third switch node (CT) for receiving the control signal and a circuit (A1, R1) connected to the third switch node (CT) and the third terminal (the base of Q0), the circuit having a sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch. Note that (A1) has very high input impedance. Transistor (Q0) can be a FET (col. 3, lines 56-57). As to the language recited on the last three lines of claim 1, it is noted that this is merely "result" language and thus cannot be relied upon to distinguish over the disclosure of Huijsing et al. ie., since the reference meets all of the claimed structure (and the functions performed by that structure), the reference meets claims 1 and 2 under 102(b). Note that apparatus claims, to be patentable over the prior art, must define over the prior art by structure, not the result of that structure.

Claims 3-5 are rejected under 35 U.S.C. 102 (b) as being anticipated by Simmons et al. (5,223,751).

Regarding claims 3-5, figure 3 of Simmons shows a transistor circuit for implementing a switch, comprising: a first switch node (the source of 42), configured to connect to an external circuit; a second switch node (46) configured to connect to the external circuit; a transistor device (42) having a first terminal connected to the first switch node a second terminal (the drain of 42) connected to the second switch node, and a third terminal (gate) configured to receive a control signal (IN) for controlling the electrical connectivity between the first terminal and the second terminal (when transistor 42 is activated); and a circuit (26) connected to the second terminal of the transistor device, the circuit configured to provide a voltage (Vr) to the second terminal (when 48 is turned on) when the control signal engages the transistor device. As to the language recited on the last three lines of claim 1, it is noted that this is merely "result" language and thus cannot be relied upon to distinguish over the disclosure of Simmons et al. ie., since the reference meets all of the claimed structure (and the functions performed by that structure), the reference meets claims 3-5 under 102(b). Note that apparatus claims, to be patentable over the prior art, must define over the prior art by structure, not the result of that structure.

Claims 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (US Pat. 4,752,703).

Regarding claims 6 and 7, figure 1 of Lin shows a transistor circuit for implementing a differential switch comprising:

a first switch node (X) configured to connect to an external circuit;

a second switch node (Y) configured to connect to the external circuit;

a first transistor (11) device having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive **a control signal (Vin)** applied to the gate of (11) that controls the electrical connectivity between the first terminal and the second terminal (when element 11 is turned on); a second transistor device (12) having a first terminal connected to the second terminal of the first transistor device (11), a second terminal connected to the second switch node (Y), and a third terminal configured to receive **the control signal (Vin)** and a third transistor device (17) having a first terminal connected to the first terminal of

the first transistor device (11), a second terminal connected to the second terminal of the second transistor device (12) via (18), and a **third terminal (gate) configured to receive the control signal (Vin)**. The first, second and third transistors are MOSFET transistors.

Regarding claim 8, it is inherent that the first, second and third transistors have parasitic capacitances (gate-source or gate drain capacitance) and their parasitic characteristics are predetermined during the phases of manufacturing.

Response to arguments

In the Remarks page 10, paragraph 1, Applicant argues that "the '747' does not disclose, or suggest that the circuit connected to the third switch node and the third terminal has a sufficiently high impedance.....and the second transistor device". In fact, the claimed circuit and the circuit of '947' have the same structure and col. 3, lines 45-46 and in col. 4, lines 43-45 disclose **a high impedance** input due to the "a circuit" (A1, R1). Thus, **inherently** this high input impedance will prevent the third switch node from functioning as an AC ground and thereby reduce the parasitic capacitance between the first and second terminal of the transistor device. Note that a transistor performs like **a switch** if the control signal is high enough to drive the transistor in the saturation mode.

In page 11, paragraph 2-3, the Applicant argues that " the '751' patent does not disclose, teach, or suggest a transistor circuit for implementing **a switch**, which comprises **first and second switch nodes**". The Applicant is respectfully reminded that a circuit described in a claim is examined by its structure, not by the **names** assigned by the Applicant because the names of a circuit and its components cannot be relied upon to distinguish over the prior art since the '751' reference meets all of the claimed structure and the function performed by that structure. Also, it is well known in the art that a transistor works like a switch. In the '751' patent, transistor (42) is turned ON and OFF hard, thus it performs like a switch.

Regarding to the '703' patent, the Applicant argues that the second terminal of the third transistor (17) is not connected to the second terminal of the second transistor device (12). In fact, the second terminal of the third transistor (17) is **connected** to the second terminal of the second transistor device (12) **via (18).** The Applicant fails to cite in the claim that the connection between two transistors is a direct connection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 746-5716. The fax phone number for this Group is (703) 308-7725.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
Examiner
08-27-02

TUAN T. LAM
PRIMARY EXAMINER